WHAT IS CLAIMED:

1. A programmable image data acquisition system, comprising:

a host computer having at least one host processor to execute operations with a host operating system and a host memory to store image data; and

a programmable detector framing node to receive image data output from an image detection system and communicate the received image data to the host memory, said detector framing node being selectably programmable by reading a programmable memory unit after power is initially applied thereto.

2. The system according to claim 1, said detector framing node further comprising:

a plurality of frame buffer memory units to store the received image data output from the image detection system; and

a control unit comprising

the programmable memory unit,

a data acquisition processor to control storage and retrieval of the image data in the frame buffer memory units, and

an event processor to execute event instructions to control the detector framing node and the image detection system.

3. The system according to claim 2, said detector framing node further comprising:

a JTAG port being connected to the programmable memory unit through a JTAG loop, such that instructions for programming the programmable memory unit are communicable to the programmable memory unit by way of the JTAG port.

4. The system according to claim 3, said detector framing node further comprising:

a computer communication interface for connecting said detector framing node to said host computer by way of a computer communication bus; and

a local bus connecting the computer communication interface to the control unit,

wherein the JTAG loop is selectably connectable to the local bus such that the programmable memory unit is programmed by way of instructions communicated by the at least one host processor over the computer communication bus, through the computer communication interface, to the local bus, and over the JTAG loop.

5. The system according to claim 2, said detector framing node communicating with the at least one host processor over the computer communication bus at a first clock frequency and receiving the image data from the image detection system at a second clock frequency different from the first clock frequency.

6. The system according to claim 5, said detector framing node communicating with the at least one host processor over the computer communication bus in parallel at the first clock frequency and receiving the image data from the image detection system in serial at the second clock frequency.

7. The system according to claim 5, wherein the first clock frequency is a PCI frequency of at least 33 MHz and the second clock frequency is a fiber optic transmission clock frequency of at least 1 GHz.

8. The system according to claim 2, wherein the event processor controls communication of event instructions to a radiation generation system for controlling generation of radiation.

9. The system according to claim 2, wherein the received image data is radioscopic image data, and the image detection system is an x-ray detection system.

10. The system according to claim 2, wherein the programmable memory unit is comprised of a plurality of daisy chained eeproms.

11. The system according to claim 10, wherein the plurality of daisy chained eeproms are selectably connected to said host computer by way of at least one JTAG loop communicating with a computer communication bus by way of a computer communication interface.

12. The system according to claim 10, wherein each of the event processor and the data acquisition processor has an associated eeprom unit, which is respectively programmable in a passive serial mode.

13. The system according to claim 1, said detector framing node further comprising:

a power on reset unit to delay application of power for booting the programmable memory unit for a predetermined time period after power is applied to said detector framing node.

14. The system according to claim 13, wherein the predetermined period of time is at least 140 msec.

15. The system according to claim 1, said detector framing node further comprising:

a JTAG port being connected to the programmable memory unit through a JTAG loop, such that instructions for programming the programmable memory unit are communicable to the programmable memory unit by way of the JTAG port.

16. The system according to claim 1, further comprising:

a computer communication interface connecting said detector framing node to said host computer by way of a computer communication bus; and

a local bus connecting the computer communication interface to the control unit,

wherein a JTAG loop communicates with the local bus such that the programmable memory unit is programmed by way of instructions communicated by the at least one host processor over the computer communication bus, through the computer communication interface, to the local bus, and over the JTAG loop.

17. The system according to claim 1, wherein the host computer operating system is a non-real time operating system.

18. The system according to claim 1, wherein the host computer operating system is a real time operating system.

19. The system according to claim 1, wherein the host computer operating system is a task based operating system.

20. The system according to claim 1, wherein the received image data is received in real time from the image detection system.

21. The system according to claim 1, said detector framing node further comprising:

a first JTAG port being connected to the programmable memory unit through a first JTAG loop, such that instructions for programming the programmable memory unit are communicable to the programmable memory unit by way of the first JTAG port; and

a second JTAG port being connected to said control unit by way of a second JTAG loop, such that instructions may be communicated to the control unit independent of communication with the programmable memory unit.

22. The system according to claim 1, said detector framing node further comprising:

a computer communication interface connecting said detector framing node to said host computer by way of a computer communication bus; and

a local bus connecting the computer communication interface to the control unit,

wherein a first JTAG loop communicates with the local bus such that the programmable memory unit is programmed by way of instructions communicated by the at least one host processor over the computer communication bus, through the computer communication interface, to the local bus, and over the JTAG loop, and

wherein a second JTAG loop communicates with said control unit such that instructions may be communicated independent of communication with the programmable memory unit.

23. The system according to claim 1,

said detector framing node further comprising a control unit comprising the programmable memory unit, a data acquisition processor to control storage and retrieval of the image data in a plurality of frame buffer memory units, and an event processor to execute event instructions to control the detector framing node and the image detection system,

the system comprising an event processor power on reset unit to delay application of power to the event processor and a data acquisition processor power on reset unit to delay application of power to the data acquisition processor.

24. The system according to claim 1, said detector framing node further comprising:

an image detection interface to receive the image data from an image detection system; and

a memory unit to store the image data received by said image detection interface before communication to the host memory.

25. The system according to claim 24, wherein the image detection interface is a fiber optic interface to receive the image data over an optical fiber data link.

26. A detector framing node, comprising:

a computer communication interface to communicate with at least one host processor over a computer communication bus according to a predetermined protocol, the at least one host processor executing operations with a host operating system and having an associated host memory to store received image data; and

a control unit to receive a plurality of event instructions from the at least one host processor through said computer communication interface for controlling events in the detector framing node, the event instructions being stored into an event queue for execution in real time at predetermined timing intervals,

wherein said control unit is selectably programmable by reading a programmable memory unit after power is applied to said detector framing node.

27. The detector framing node according to claim 26, further comprising:

a plurality of frame buffer memory units to store received image data output from an image detection system; and

said control unit comprising a data acquisition processor to control storage and retrieval of the image data in the frame buffer memory units.

28. The detector framing node according to claim 26, said detector framing node further comprising:

a JTAG port being connected to the programmable memory unit through a JTAG loop, such that instructions for programming the programmable memory unit are communicable to the programmable memory unit by way of the JTAG port.

29. The detector framing node according to claim 28, further comprising:

a local bus connecting the computer communication interface to the control unit,

wherein the JTAG loop communicates with the local bus such that the programmable memory unit is selectively programmed by way of instructions communicated by the at least one host processor over the computer communication bus, through the computer communication interface, to the local bus, and over the JTAG loop.

30. The detector framing node according to claim 26, wherein communication over the computer communication bus is conducted at a first clock frequency and image data is received from an image detection system at a second clock frequency different from the first clock frequency.

31. The detector framing node according to claim 30, wherein communication over the computer communication bus is conducted in parallel at the first clock frequency and the image data is received from the image detection system in serial at the second clock frequency.

32. The detector framing node according to claim 30, wherein the first clock frequency is a PCI frequency of at least 33 MHz and the second clock frequency is a fiber optic transmission clock frequency of at least 1 GHz.

33. The detector framing node according to claim 26, wherein the control unit controls communication of event instructions to a radiation generation system for controlling generation of radiation.

34. The detector framing node according to claim 26, further comprising:

an image detection interface to receive the image data from an image detection system; and

a memory unit to store the image data received by said image detection interface before communication to the host memory.

35. The detector framing node according to claim 34, wherein the image data is radioscopic image data and the image detection system is an x-ray detection system.

36. The detector framing node according to claim 26, wherein the programmable memory unit is comprised of a plurality of daisy chained eeproms.

37. The detector framing node according to claim 36, wherein the plurality of daisy chained eeproms are selectably programmable by way of transfer of programming instructions from the host computer to the detector framing node memory unit, and then through transfer from the detector framing node memory unit to the eeproms by way of the data acquisition processor.

38. The detector framing node according to claim 36, wherein said control unit includes an event processor and a data acquisition processor, each having a respectively associated eeprom unit.

39. The detector framing node according to claim 36, wherein each of the eeproms is programmable in a passive serial mode.

40. The detector framing node according to claim 26, further comprising:

a power on reset unit to delay application of control signals for booting the programmable memory unit for a predetermined time period after power is applied to the detector framing node.

41. The detector framing node according to claim 40, wherein the predetermined period of time is at least 140 msec.

42. The detector framing node according to claim 26, further comprising:

a JTAG port being connected to the programmable memory unit through a JTAG loop, such that instructions for programming the programmable memory unit are communicable to the programmable memory unit by way of the JTAG port.

43. The detector framing node according to claim 26, further comprising:

a local bus connecting the computer communication interface to the control unit,

wherein a JTAG loop communicates with the local bus such that the programmable memory unit is programmed by way of instructions communicated by the at least one host processor over the computer communication bus, through the computer communication interface, to the local bus, and over the JTAG loop.

44. The detector framing node according to claim 26, wherein the received image data is received in real time from the image detection system.

45. The detector framing node according to claim 26, further comprising:

a first JTAG port being connected to the programmable memory unit through a first JTAG loop, such that instructions for programming the programmable memory unit are communicable to the programmable memory unit by way of the first JTAG port; and

a second JTAG port being connected to said control unit by way of a second JTAG loop, such that instructions to said control unit may be communicated independent of communication with the programmable memory unit.

46. The detector framing node according to claim 26, further comprising:

a local bus connecting the computer communication interface to the control unit,

wherein a first JTAG loop communicates with the local bus such that the programmable memory unit is programmed by way of instructions communicated by the at least one host processor over the computer communication bus, through the computer communication interface, to the local bus, and over the JTAG loop, and

wherein a second JTAG loop communicates with said control unit such that instructions may be communicated independent of communication with the programmable memory unit.

47. The detector framing node according to claim 26, further comprising:

a data acquisition processor to control storage and retrieval of the image data in a plurality of frame buffer memory units;

an event processor power on reset unit to delay application power to an event processor controlling the event queue upon reset of the detector framing node; and

a data acquisition processor power on reset unit to delay application of power to the data acquisition processor upon reset of the detector framing node.

48. The detector framing node according to claim 26, further comprising:

an image detection interface to receive the image data from an image detection system; and

a memory unit to store the image data received by said image detection interface before communication to the host memory.

49. The detector framing node according to claim 48, wherein the image detection interface is a fiber optic interface to receive the image data over an optical fiber data link.

50. A programmable detector framing node, comprising:

a computer communication interface to communicate with a host computer having at least one host processor and a host memory;

a detector framing node memory unit to store data for processing within the detector framing node; and

a control unit connected to said computer communication interface and to said detector framing node memory unit by a local bus, said control unit to control storage of data transferred from the computer communication interface into the detector framing node memory unit, said control unit comprising a programmable memory unit to store initial boot sequence instructions and to load the initial boot

sequence instructions for execution by said control unit upon reset or initial application of power to the detector framing node,

wherein the initial boot sequence instructions are updated by communicating update instructions from the host computer through the computer communication interface and into said detector framing node memory unit, before transfer from said detector framing node memory unit to the programmable memory unit.

51. The programmable detector framing node according to claim 50, further comprising:

a JTAG loop communicating data between the local bus and the programmable memory unit,

wherein the update instructions are communicated from the local bus across the JTAG loop during updating.